


MyeSrsForm PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-2473	SERIAL NO. Filed Herewith
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				FILING DATE Filed Herewith	GROUP Unassigned
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)					
	AA		Ono, K. et al., "Analysis of Current-Voltage Characteristics in Polysilicon TFTs for LCDs", IEDM Tech. Digest, 1988, pp. 256-259.		
	AB		Yamauchi, N. et al., "Drastically Improved Performance in Poly-Si TFTs with Channel Dimensions Comparable to Grain Size", IEDM Tech. Digest, 1989, pp. 353-356.		
X	AC		King, T. et al., "A Low-Temperature ($\leq 550^\circ\text{C}$) Silicon-Germanium MOS Thin-Film Transistor Technology for Large-Area Electronics", IEDM Tech. Digest, 1991, pp. 567-570. not readable.		
X	AD		Kuriyama, H. et al., "High Mobility Poly-Si TFT by a New Excimer Laser Annealing Method for Large Area Electronics", IEDM Tech. Digest, 1991, pp. 563-566. not readable.		
	AE		Jeon, J. et al., "A New Poly-Si TFT with Selectively Doped Channel Fabricated by Novel Excimer Laser ... Annealing", IEDM Tech. Digest, 2000, pp. 213-216.		
X	AF		Kim, C.H. et al., "A New High Performance Poly-Si TFT by Simple Excimer Laser Annealing on Selectively Floating a-Si Layer", IEDM Tech. Digest, 2001, pp. 751-754. not readable.		
	AG		Hara, A. et al., "Selective Single-Crystalline-Silicon Growth at the Pre-Defined Active Regions of TFTs on a Glass by a Scanning CW Laser Irradiation", IEDM Tech. Digest, 2000, pp. 209-212.		
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	AK		Kesan, V. et al., "High Performance 0.25 μm p-MOSFETs with Silicon-Germanium Channels for 300K and 77K Operation", IEDM Tech. Digest, 1991, pp. 25-28.		
	AL		Garone, P.M. et al., "Mobility Enhancement and Quantum Mechanical Modeling in Ge ₂ Si ₃ Channel MOSFETs from 90 to 300K", IEDM Tech. Digest, 1991, pp. 29-32.		
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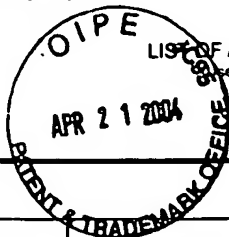
Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-2473	SERIAL NO. Filed Herewith
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)					
	AM		Feder, B.J., "I.B.M. Finds Way to Speed Up Chips", The New York Times, June 8, 2001, reprinted from		
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	AN		Rim, K. et al., "Strained Si NMOSFET's for High Performance CMOS Technology", 2001 Sympos. on VLSI Tech.		
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	AO		Li, P. et al., "Design of High Speed Si/SiGe Heterojunction Complementary MOSFETs with Reduced Short-Channel		
			Effects", Natl. Central University, ChungLi, Taiwan, ROC, Aug. 2001, Contract No. NSC 89-2215-E-008-049, National Science Council of Taiwan., pp. 1, 9.		
	AP		Ernst, T. et al., "Fabrication of a Novel Strained SiGe:C-channel Planar 55 nm nMOSFET for High-Performance		
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	AQ		Rim, K. et al., "Characteristics and Device Design of Sub-100 nm Strained SiN- and PMOSFETs", 2002 Sympos.		
			on VLSI Tech. Digest of Technical Papers, pp. 98-99. <i>not readable.</i>		
	AR		Bellford, R.E. et al., "Performance-Augmented CMOS Using Back-End Uniaxial Strain", DRC Conf. Digest, 2002,		
			pp. 41-42.		
	AS		Shima, M. et al., "<100> Channel Strained-SiGe p-MOSFET with Enhanced Hole Mobility and Lower Parasitic		
			Resistance", 2002 Sympos. on VLSI Tech. Digest of Technical Papers, pp. 94-95.		
	AT		Nayfeh, H.M. et al., "Electron Inversion Layer Mobility in Strained-Si n-MOSFET's with High Channel Doping		
			Concentration Achieved by Ion Implantation", DRC Conf. Digest, 2002, pp. 43-44.		
	AU		Bae, G.J. et al., "A Novel SiGe-Inserted SOI Structure for High Performance PDSOI CMOSFET", IEDM Tech.		
			Digest, 2000, pp. 667-670.		
	AV		Cheng, Z. et al., "SiGe-on-Insulator (SGOI): Substrate Preparation and MOSFET Fabrication for Electron Mobility		
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	AW		Huang, L.J. et al., "Carrier Mobility Enhancement in Strained Si-on-Insulator Fabricated by Wafer Bonding", 2001		
			Sympos. on VLSI Tech. Digest of Technical Papers, pp. 57-58.		
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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2473	SERIAL NO. Filed Herewith
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)					
	AX		Mizuno, T. et al., "High Performance CMOS Operation of Strained-SOI MOSFETs Using Thin Film SiGe-on-Insulator Substrate", 2002 Sympos. on VLSI Tech. Digest of Technical Papers, p. 106-107.		
	AY		Tezuka, T. et al., "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique", 2002 VLSI Tech. Digest of Technical Papers, pp. 96-97.		
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	BB		Markoff, J., "I.B.M. Circuits are Now Faster and Reduce Use of Power", The New York Times, Feb. 25, 2002, reprinted 3/20/02 from http://story.news.yahoo.com/news?tmpl=story&u=nyt/20020225/... , 1 pg.		
	BC		Park, J.S. et al., "Normal Incident SiGe/Si Multiple Quantum Well Infrared Detector", IEDM Tech. Digest, 1991, pp. 749-752.		
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	BF		Myers, S.M. et al., "Deuterium Interactions in Oxygen-Implanted Copper", J. Appl. Phys., Vol. 65(1), Jan. 1, 1989, p. 311-321.		
	BG		Saggio, M. et al., "Innovative Localized Lifetime Control in High-Speed IGBTs", IEEE Elec. Dev. Lett., V. 18, No. 7, July 1997, pp. 323-325.		
	BH		Lu, N.C.C. et al., "A Buried Trench DRAM Cell Using a Self-Aligned Epitaxy Over Trench Technology", IEDM Tech. Digest, 1988, pp. 568-591.		
	BI		Yamada, T. et al., "Spread Source/Drain (SSD) MOSFET Using Selective Silicon Growth for 64Mbit DRAMs", IEDM Tech. Digest, 1989, pp. 35-38.		
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	BJ		van Meer, H. et al., "Ultra-Thin Film Fully-Depleted SOI CMOS with Raised G/S/D Device Architecture for Sub-100		
			nm Applications", 2001 IEEE Intematl. SOI Conf. 10/01, pp. 45-46.		
	BK				
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EXAMINER <i>J. Mondt</i>			DATE CONSIDERED <i>09/07/05</i>		
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U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
MI22-2473SERIAL NO.
10760,087LIST OF ART CITED BY APPLICANT
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Arup BhattacharyyaFILING DATE
January 14, 2004GROUP
Unknown

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
<i>[Signature]</i>	AA	4,692,994	09/87	Moniwa et al.			
<i>[Signature]</i>	AB	4,768,076	08/88	Aoki et al.			
<i>[Signature]</i>	AC	5,006,913	04/91	Sugahara et al.			
	AD						
	AE						
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FOREIGN PATENT DOCUMENTS

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U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
UP	AA	6,429,085 B1	08/02	Plinter			
	AB						
	AC						
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